Our Docket No.: 00-332 / 1496.00075

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	David Neil Pether et al.		
Application No.:	09/739,956	Examiner:	Arnold, A.
Filed:	December 19, 2000	Art Group:	2697
For:	GENERATION OF GRAPHICS IN COMPUTER SYSTEMS		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 13, 2003.

By: Mary Donna Berkley
Mary Donna Berkley

APPEAL BRIEF

Mail Stop - Appeal Brief Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Please charge $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(f) and any additional fees or credit any overpayment to Deposit Account Number 12-2252.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, LSI Logic Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 3-11 and 13-30 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1, 3-11 and 13-30.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on March 26, 2003. On June 26, 2003 the Appellants filed a Notice of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns an apparatus (10) for generating a region of graphics on a display. The apparatus generally comprises a bus (16), a plurality of registers (24, 26), a memory (14), a calculation circuit (30) and a control circuit (36). The bus may have a first address range and a second address range. The registers may be within the first address range and configured to store an X coordinate (X) and a Y coordinate (Y) of a pixel to be drawn on the display. The

memory may be within the second address range. The calculation circuit may be configured to calculate an address (MEMORY ADDR.) in the second address range for storage of data (DATA) corresponding to the pixel in dependence on the X and the Y coordinates. The control circuit may be configured to control writing of the data in the memory at the address.

VI. ISSUES

The first issue is whether claims 1, 3, 20 and 30 are patentable under 35 U.S.C. §102(b) over Lee et al., U.S. Patent No. 5,214,753 (hereafter Lee).

The second issue is whether claims 4 and 5 are patentable under 35 U.S.C. §103(a) over Lee in view of Ashburn, U.S. Patent No. 5,651,106.

The third issue is whether claims 6 and 21 are patentable under 35 U.S.C. §103(a) over Lee in view of "Basic Raster Graphics Algorithms for Drawing 2D Primitives" by Foley.

The fourth issue is whether claims 7 and 22 are patentable under 35 U.S.C. §103(a) over Lee in view of Krenik et al., U.S. Patent No. 5,699,087 (hereafter Krenik).

The fifth issue is whether claims 8-10 and 23-24 are patentable under 35 U.S.C. §103(a) over Lee in view of Krenik and Chiu et al., U.S. Patent No. 5,796,391 (hereafter Chiu).

The sixth issue is whether claims 11, 13, 25 and 26 are patentable under 35 U.S.C. §103(a) over Lee in view of Prouty, U.S. Patent No. 5,986,658.

The seventh issue is whether claim 14 is patentable under 35 U.S.C. §103(a) over Lee in view of Prouty, Krenik and Chiu.

The eighth issue is whether claims 15-19 and 27-29 are patentable under 35 U.S.C. §103(a) over Lee in view of Ozcelik et al., Patent Publication No. 2002/0149626 (hereafter Ozcelik).

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1, 20 and 30 stand together.

Group 2: Claim 3 stands alone.

Group 3: Claim 4 stands alone.

Group 4: Claim 5 stands alone.

Group 5: Claims 6 and 21 stand together.

Group 6: Claims 7 and 22 stand together.

Group 7: Claims 8-10, 23 and 24 stand together.

Group 8: Claims 11, 13, 25 and 26 stand together.

Group 9: Claim 14 stands alone.

Group 10: Claim 15 stands alone.

Group 11: Claims 16 and 27 stand together.

Group 12: Claims 17 and 28 stand together.

Group 13: Claims 18 and 29 stand together.

Group 14: Claim 19 stands alone.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. 35 U.S.C. § 102

The Federal Circuit has stated that "[t]o anticipate, *every element and limitation* of the claimed invention must be found in a single prior art reference, *arranged as in the claim.*"[1] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[3]

Selected groupings of the claims are each patentable over Lee

1. Group 1 (claims 1, 20 and 30) is fully patentable over Lee

The group 1 claims provide a bus having a first address range and a second address range. Despite the assertion by the Examiner, column 22, lines 1-8 of Lee appear to be silent regarding a bus having two address ranges.[4] The text of Lee cited by the Examiner reads:

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[3] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

[4] Office Action, March 26, 2003, page 2, section 2, lines 2-4.

> The busses 422 and 424 carry data and address information from the host CPU are coupled to one set of inputs of the multiplexer. A data bus 428 and an address bus 430 are coupled to another set of inputs. The multiplexer 426 selects either the pair of busses 428 and 430 or the pair of busses 424 and 422 for coupling, respectively, to data and address output busses 432 and 434.

Nowhere in the above text, or in any other section, does Lee appear to state that any of the four busses 422, 424, 428 or 430 have two address ranges. Therefore, the Examiner has failed to establish that Lee discloses or suggests a bus having a first address range and a second address range as presently claimed.

The group 1 claims further provide storing an X coordinate and a Y coordinate of a pixel in the first address range. Despite the assertion by the Examiner, column 8, lines 19-23 of Lee appear to be silent regarding storing the X and Y coordinates on one of the busses 422, 424, 428 or 430.[5] The text of Lee cited by the Examiner reads:

> Simultaneously, the value X_1 on bus 48 is latched into a current-X-left register (not shown) inside the accumulator-left circuit 60.
>
> At time 5, the scan line number Y_2 for the scan line passing through the vertex 66 in FIG. 6 is loaded into the Y_L register 38 and resides on the input data bus 44.

The above text states that the current-X-left register is on the bus 48 and the Y_L register 38 is on the bus 44. Therefore, the current-X-left register and the Y_L register 38 are not on the same bus. Furthermore, the current-X-left register and the Y_L register 38 do not appear to be on any of the busses 422, 424, 428 or 430 cited by the Examiner for the claimed bus. Therefore, the Examiner has failed to establish that Lee discloses or suggest storing an X coordinate and a Y coordinate of a pixel in a first address range as presently claimed.

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[5] Office Action, March 26, 2003, page 2, section 2, lines 4-5.

The group 1 claims further provide (i) a memory within the second address range and (ii) calculating an address in the second address range of the bus for storage of data corresponding to the pixel in dependence on the X and the Y coordinates. The Examiner cited a RAM 420 of Lee as anticipating the claimed memory.[6] The Examiner further cited column 17, lines 59-63 of Lee for calculating an address directed to the RAM 420.[7] The text of Lee cited by the Examiner reads:

> The values of X_1 and X_3 are sent to the address calculation circuit 336 via a bus 344 and they are sent to the interpolation circuits 332 and 334 via the buses 346 and 348, respectively, through tri-state buffers 350 and 352, respectively.

Nowhere in the above text, or any in other section, does Lee appear to state that the address calculation circuit 336 generates an address within an address range of the RAM 420. Furthermore, the RAM 420 does not appear to be one of the busses 422, 424, 428 or 430. Therefore, the Examiner has failed to establish that Lee discloses or suggests a memory within a second address range and calculating an address in the second address range for storage of data corresponding to a pixel in dependence on an X and Y coordinates as presently claimed.

The group 1 claims further provide controlling writing of the data in the memory at the address. Despite the assertion by the Examiner, column 18, lines 30-34 and a control logic block 33 in FIG. 1A of Lee appear to be silent regarding write control to the RAM 420.[8] The text of Lee cited by the Examiner reads:

> Also, control signals are sent on bus 356 to cause the address calculation circuit to begin calculating the addresses in the frame buffer that correspond in the bit map to the pixels along the line 360 in FIG. 6.

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[6] Office Action, March 26, 2003, page 2, section 2, lines 5-6.

[7] Office Action, March 26, 2003, page 2, section 2, lines 6-7.

[8] Office Action, March 26, 2003, page 2, section 2, lines 7-9.

Nowhere in the above text, or in any other section, does Lee appear to indicate that the control logic block 33 controls writing of data to the RAM 420. Furthermore, bus 356 mentioned above in FIG. 9A of Lee has no clear relationship to the control logic block 33 in FIG. 1A of Lee. Therefore, the Examiner has failed to establish that Lee discloses or suggests controlling writing of data in a memory at an address as presently claimed.

In summary, the Examiner has failed to establish that Lee discloses or suggest (i) a bus having a first address range and a second address range, (ii) storing coordinates within the first address range, (iii) a memory within the second address range, (iv) calculating an address in the second address range and (v) controlling writing of the data in the memory at the address as arranged in the present claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

2. Group 2 (claim 3) is fully patentable over Lee

Claim 3 depends directly from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 (group 1) are incorporated hereunder in support of group 2.

Claim 3 further provides a clipping circuit generating a clipping signal configured to indicate that at least one of the X and the Y coordinates falls outside a predetermined clipping limit. Despite the assertion by the Examiner, column 15, lines 22-26 of Lee appear to be silent regarding generation of a signal indicating a clip.[9] The text of Lee cited by the Examiner reads:

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[9] Office Action, March 26, 2003, page 2, section 2, lines 10-12.

> The function of the math pipeline is to take the list of objects defined by the user and perform matrix math operations to rotate, scale, translate, clip and project the object and output a 2-D list of vertices in screen coordinates.

Nowhere in the above text, or in any other section, does Lee appear to indicate that the math pipeline circuit 310 in FIG. 9B generates a clipping signal. Therefore, the Examiner has failed to establish that Lee discloses or suggests a clipping circuit generating a clipping signal configured to indicate that at least one of an X and a Y coordinates falls outside a predetermined clipping limit as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be reversed.

B. **35 U.S.C. § 103**

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[10] "[T]he factual inquiry whether to combine references must be thorough and searching."[11] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[12] "It must be based on objective evidence of record."[13] The Examiner must show that (a) there is some suggestion or motivation, either in the references or

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[10] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[11] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[12] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[13] *Id.* at 1343, 61 USPQ2d at 1434.

in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[14] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[15]

Selected groupings of the claims are each patentable over Lee and Ozcelik

1. Group 10 (claim 15) is fully patentable over Lee in view of Ozcelik

Claim 15 provides (i) a register accessible via a bus for storing coordinates of a pixel to be drawn on a display and (ii) a memory accessible via the bus for storage of data corresponding to the pixel. Despite the assertion by the Examiner, column 18, lines 25-30 of Lee appear to be silent regarding a register and a memory on a bus.[16] The text of Lee cited by the Examiner reads:

> Simultaneously, the microcode and video display processor combine to put control signals on a bus 356 to the address calculation circuit 336 so as to cause the address calculation circuit to load these two horizontal position values in internal registers used to store the intersection points for scan lines.

Nowhere in the above text, or in any other section, does Lee appear to indicate that the internal register of the address calculation circuit 336 and an unidentified memory are accessible on the same bus. The above text may indicate that the address calculation circuit 336 may access its internal

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[14] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003 §2142.

[15] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

[16] Office Action, March 26, 2003, page 9, section 10, lines 2-3.

registers, but is silent regarding the internal registers being accessible via the bus 356. Therefore, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest a register accessible via a bus for storing coordinates of a pixel to be drawn on a display and a memory accessible via the bus for storage of data corresponding to the pixel as presently claimed.

Claim 15 further provides a control circuit for controlling the register and a calculation circuit to cause the data (corresponding to the pixel) to be stored in the memory at the address. In contrast, the Examiner has not provided any evidence or arguments that Lee and/or Ozcelik teach or suggest a control circuit for controlling a register and a calculation circuit to cause data corresponding to a pixel to be stored in a memory at an address as presently claimed.

Furthermore, the Examiner has failed to establish *prima facie* obviousness to combine the references. The Examiner has asserted that motivation to combine is "to reduce complexity and increase flexibility in defining displays." per paragraph 8 of Ozcelik.[17] The text of Ozcelik cited by the Examiner reads:

> Thus, there is a need for a display hardware that has a relatively low hardware complexity yet provides substantial flexibility in defining displays.

The asserted motivation appears to contradict with the asserted combination. Adding additional capabilities to the address calculation circuit 336 of Lee does not necessarily reduce circuit complexity. To the contrary, adding functionality commonly involves increasing circuit complexity to perform the new functions. No explanation has been provided by the Examiner how adding capabilities could cause a reduction in complexity. Therefore, the "reducing complexity" argument appears to be nothing more than a conclusory statement. Regarding the "flexibility" argument, no

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[17] Office Action, March 26, 2003, page 9, section 10, lines 10-11.

evidence has been provided that one of ordinary skill in the art would view Ozcelik as a means for *increasing* flexibility in defining displays as compared with what Lee already teaches. In particular, the cited text of Ozcelik only states that there is a need for *substantial* flexibility. However, no evidence has been provided that Lee teaches something less than substantial flexibility which one of ordinary skill in the art would thus be motivated to increase. The assertion by the Examiner that Ozcelik would increase a flexibility of Lee is speculative and lacks support evidence. Thus, the Examiner has failed to establish *prima facie* obviousness to combine the references for lack of clear and particular evidence for motivation.

In summary, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest (i) a register accessible via a bus for storing coordinates of a pixel to be drawn on a display and a memory accessible via the bus for storage of data corresponding to the pixel and (ii) a control circuit for controlling the register and a calculation circuit to cause the data corresponding to the pixel to be stored in the memory at the address as presently claimed. The Examiner has also failed to provide clear and particular evidence of motivation to combine the references. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

2. Group 11 (claims 16 and 27) is fully patentable over Lee in view of Ozcelik

The group 11 claims depend from the group 10 and the group 1 claims and thus contains all of the limitations of the group 10 and the group 1 claims, respectively. Consequently, the arguments presented above in support of the patentability of group 10 (for claim 16) and group 1 (for claim 27) are incorporated hereunder in support of group 11.

The group 11 claims further provide storing data in a single memory word prior to the single memory word being written to the address in the memory (calculated by the calculation circuit). The Examiner has asserted that column 23, lines 58-61 of Lee teach the claim language.[18] The text of Lee cited by the Examiner reads:

> The T_1 attribute stored in register 494 and the T_2 attribute stored in register 496 are output on busses 500 and 502, respectively, to multiplexers 504 and 506, respectively.

Nowhere in the above text, or in any other section, does Lee appear to state that the data stored in the registers 494 and 496 is written to (i) the RAM 420 or (ii) an address calculated by the address calculation circuit 336. Therefore, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest storing data in a single memory word prior to the single memory word being written to an address in an memory calculated by an calculation circuit as presently claimed. As such, claims 16 and 27 are fully patentable over the cited references and the rejection should be reversed.

3. Group 12 (claims 17 and 28) is fully patentable over Lee in view of Ozcelik

The group 12 claims depend from the group 11 and the group 1 claims and thus contains all of the limitations of the group 11 and the group 1 claims, respectively. Consequently, the arguments presented above in support of the patentability of group 11 (for claim 17) and group 1 (for claim 28) are incorporated hereunder in support of group 12.

The group 12 claims further provide combining data for at least two pixels to be drawn in dependence on a word address of each of the pixels to permit storage of the data for the

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[18] Office Action, March 26, 2003, page 9, section 10, lines 15-16.

pixels in a single memory word. Contrary to the assertion by the Examiner, column 23, lines 58-61 of Lee appear to be silent regarding combining two pixels.[19] The text of Lee cited by the Examiner reads:

> The T_1 attribute stored in register 494 and the T_2 attribute stored in register 496 are output on busses 500 and 502, respectively, to multiplexers 504 and 506, respectively.

Nowhere in the above text, or in any other section, does Lee appear to indicate that the pixels stored in the registers 494 and 496 are combined in dependence on a word address of each of the pixels. Therefore, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest combining data for at least two pixels to be drawn in dependence on a word address of each of the pixels to permit storage of the data for the pixels in a single memory word as presently claimed. As such, claims 16 and 28 are fully patentable over the cited references and the rejection should be reversed.

4. Group 13 (claims 18 and 29) is fully patentable over Lee in view of Ozcelik

The group 13 claims depend from the group 12 claims and thus contains all of the limitations of the group 12 claims. Consequently, the arguments presented above in support of the patentability of group 12 are incorporated hereunder in support of group 13.

The group 13 claims further provide comparing word addresses of consecutive pixels to be drawn. Despite the assertion by the Examiner, column 28, lines 11-13 of Lee appear to be silent regarding comparing word addresses. The text of Lee cited by the Examiner reads:

> Further, comparator could be used to verify when all required calculations for an edge have been completed.

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[19] Office Action, March 26, 2003, page 10, lines 2-3.

Nowhere in the above text, or in any other section, does Lee appear to state that word addresses are compared. Therefore, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest comparing word addresses of consecutive pixels to be drawn as presently claimed. As such, claims 18 and 29 are fully patentable over the cited references and the rejection should be reversed.

5. **Group 14 (claim 19) is fully patentable over Lee in view of Ozcelik.**

Claim 19 depends from claim 18 and thus contains all of the limitations of claim 18. Consequently, the arguments presented above in support of the patentability of claim 18 (group 13) are incorporated hereunder in support of group 14.

Claim 19 further provides that the control circuit is configured to combine the data for the pixels. Contrary to the assertion by the Examiner, column 23, lines 63-68 of Lee appear to be silent regarding combining data for pixels.[20] The text of Lee cited by the Examiner reads:

> If a particular polygon is to be texture mapped, as indicated by information in the display list, the multiplexers 504 and 506 are controlled by signals on the control bus to select the input data on busses 500 and 502 for coupling to the output busses 511 and 512, respectively.

The above text discusses busses and multiplexers but not a control type of circuit. Furthermore, nowhere in the above text, or in any other section, does Lee appear to indicate that pixel data is combined. Therefore, the Examiner has failed to establish that Lee and Ozcelik, alone or in combination, teach or suggest a control circuit configured to combine data for pixels as presently

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[20] Office Action, March 26, 2003, page 10, lines 9-10.

claimed. As such, claim 19 is fully patentable over the cited references and the rejection should be reversed.

Selected groupings of the claims are each patentable over Lee and Ashburn

6. Group 3 (claim 4) is fully patentable over Lee in view of Ashburn

Claim 4 depends from claim 3 and thus contains all of the limitations of claim 3. Consequently, the arguments presented above in support of the patentability of claim 3 (group 2) are incorporated hereunder in support of group 3.

Claim 4 further provides that the control circuit is configured to inhibit writing of the data to the address in response to the clipping signal. In contrast, the assertion by the Examiner that column 8, lines 29-31 of Ashburn teach a control circuit attached to a clipping unit to inhibit writing data to memory appears to be incorrect. The text of Ashburn cited by the Examiner reads:

> Operations of the right stack 79 are controlled by a right stack control unit 83. The right stack performs lighting, clipping, and plane equation calculations.

Nowhere in the above text, or in any other section, does Ashburn appear to state that the right stack control unit 83 inhibits writing to the RAM 420 or any other memory. Therefore, the Examiner has failed to establish that Lee and Ashburn, alone or in combination, teach or suggest a control circuit configured to inhibit writing of data to an address in response to a clipping signal as presently claimed.

Furthermore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence for a reasonable expectation of success and for motivation to combine. In particular, the

Examiner has stated that motivation exists to "increase performance levels in graphics systems."[21] However, no evidence has been provided by the Examiner from either reference or knowledge commonly available to one of ordinary skill in the art that increased performance levels might be expected if the asserted modifications were made. The Examiner appears to be speculating on a performance improvement for the proposed combination to create a motivation. Therefore, the asserted motivation is merely a conclusory statement relying on an unsupported expectation of success lacking clear and particular evidence. As such, claim 4 is fully patentable over the cited references and the rejection should be reversed.

7. Group 4 (claim 5) is fully patentable over Lee in view of Ashburn

Claim 5 depends from claim 3 and thus contains all of the limitations of claim 3. Consequently, the arguments presented above in support of the patentability of claim 3 (group 2) are incorporated hereunder in support of group 4.

Claim 5 provides that the control circuit is configured to prevent calculation of the address in response to the clipping signal. Despite the assertion by the Examiner, column 8, lines 29-31 of Ashburn appear to be silent regarding preventing a calculation of an address.[22] The text of Ashburn cited by the Examiner reads:

> Operations of the right stack 79 are controlled by a right stack control unit 83. The right stack performs lighting, clipping, and plane equation calculations.

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[21] Office Action, March 26, 2003, page 3, section 4, line 9.

[22] Office Action, March 26, 2003, page 3, section 4, line 15.

Nowhere in the cited text, or in any other section, does Ashburn appear to indicate that the right stack control unit 83 can prevent an address calculation. Therefore, Lee and Ashburn, alone or in combination, do not appear to teach or suggest a control circuit configured to prevent calculation of an address in response to a clipping signal as presently claimed. As such, claim 5 is fully patentable over the cited references and the rejection should be reversed.

Selected groupings of the claims are each patentable over Lee and Foley

8. Group5 (claims 6 and 21) is fully patentable over Lee in view of Foley

The group 5 claims depend from the group 1 claims and thus contains all of the limitations of the group 1 claims. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 5.

The group 5 claims further provide discarding data when at least one of the X and the Y coordinates fall outside predetermined clipping limits. In contrast, the Examiner argues that Foley teaches not displaying pixels outside a clip region.[23] However, not displaying a pixel on a display provides no indication if the pixel data is kept or discarded within the graphics apparatus driving the display. Just because a user cannot see the pixel does not necessarily mean that the pixel data has been discarded. Therefore, the Examiner has failed to established that Lee and Foley, alone or in combination, teach or suggest discarding data when at least one of an X and a Y coordinate fall outside predetermined clipping limits as presently claimed. As such, claims 6 and 21 are fully patentable over the cited references and the rejection should be reversed.

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[23] Office Action, March 26, 2003, page 4, section 5, lines 5-8.

Selected groupings of the claims are each patentable over Lee and Krenik

9. Group 6 (claims 7 and 22) is fully patentable over Lee in view of Krenik

The group 6 claims depend from the group 1 claims and thus contains all of the limitations of the group 1 claims. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 6.

The group 6 claims further provide (i) memory mapping a first register storing the X coordinate to a first location and a second location in the first address range and (ii) memory mapping a second register storing the Y coordinate to a third location and a fourth location in the first address range. Contrary to the assertion by the Examiner, column 10, lines 30-34 of Krenik appear to be silent regarding memory mapping registers to multiple locations.[24] The text of Krenik cited by the Examiner reads:

> a memory having a plurality of locations for storing data and operable to provide a selected portion of said data from a selected one of said locations on a plurality of memory bitlines upon the receipt of an address corresponding to said selected location.

Nowhere in the above text, or in any other section, does Krenik appear to indicate that registers may be memory mapped to multiple locations. Even if the video RAM 20 from Krenik were to be viewed as a collection of multiple registers, nothing is inherent to an arrangement of the video RAM 20 wherein at least two of the registers are each mapped to multiple locations. Therefore, the Examiner has failed to establish that Lee and Krenik, alone or in combination, teach or suggest memory mapping a first register storing an X coordinate to a first location and a second location in a first address range and memory mapping a second register storing a Y coordinate to a third location and a fourth location in the first address range as presently claimed.

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[24] Office Action, March 26, 2003, page 5, lines 3-4.

Furthermore, the Examiner has failed to establish *prima facie* obviousness. In particular, the Examiner has asserted that motivation to combine the references exists because "this type of memory accessing procedure is conventional".[25] However, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[26] The Examiner has not provided any evidence of motivation for one of ordinary skill in the art to actually modify Lee with Krenik. Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence of motivation to combine the references. As such, claims 7 and 22 are fully patentable over the cited references and the rejections should be reversed.

Selected groupings of the claims are each patentable over Lee, Krenik and Chiu

10. Group 7 (claims 8-10, 23 and 24) is fully patentable over Lee in view of Krenik and Chiu

The group 7 claims depend from the group 6 claims and thus contains all of the limitations of the group 6 claims. Consequently, the arguments presented above in support of the patentability of group 6 are incorporated hereunder in support of group 7.

The group 7 claims further provide monitoring the first, the second, the third and the fourth memory locations for a write. Despite the assertion by the Examiner, column 3, lines 45-49 and elements 122 and 206 in FIG. 2 of Chiu appear to be silent regarding monitoring memory

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[25] Office Action, March 26, 2003, page 5, lines 7-8.

[26] M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

locations for a write. Element 122 of Chiu is a two-conductor control bus.[27] Element 206 of Chiu is an address decoder.[28] The text of Chiu cited by the Examiner reads:

> Address decoder 206 is a binary decoder which produces a load signal on one of four outputs by decoding a two-bit CONTROL signal from decoder 108. The load signals load data from bus 120 into one of the latches 202, 208, 212 and 216.

Nowhere in the above text, or in any other section, does Chiu appear to mention that the address decoder 206 monitors for writes. If anything, the address decoder 206 of Chiu appears to cause writes into the latches 202, 208, 212, and 216 instead of monitoring for the writes. Therefore, the Examiner has failed to show that Lee, Krenik and Chiu, alone or in combination, teach or suggest monitoring a first, a second, a third and a fourth memory locations for a write as presently claimed.

Furthermore, the Examiner has failed to establish *prima facie* obviousness. In particular, the Examiner argues motivation to combine the references is that (i) address decoders are conventional and (ii) the address decoder allows the registers to be translated into a memory location.[29] Regarding the "conventional"argument, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[30] The Examiner has failed to provide evidence for motivation to actually make the combination. The "translation" argument appears to be a conclusory statement since conventional address decoders are operational to decode, not translate. Therefore, the Examiner has not established *prima facie* obviousness for lack of clear and

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[27] Chiu, column 2, line 33.

[28] Chiu, FIG. 2.

[29] Office Action, March 26, 2003, page 5, section 7, lines 7-10.

[30] M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

particular evidence to combine the references. As such, claims 8-10, 23 and 24 are fully patentable over the cited references and the rejection should be reversed.

Selected groupings of the claims are each patentable over Lee and Prouty

11. Group 8 (claims 11, 13, 25 and 26) is fully patentable over Lee in view of Prouty

The group 8 claims depend from the group 1 claims and thus contains all of the limitations of the group 1 claims. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 8.

The Examiner has failed to establish *prima facie* obviousness to combine Lee and Prouty to achieve the group 8 claims. In particular, the Examiner has asserted that motivation to combine is to "provide for drawing complex line styles in real time."[31] However, the Examiner has not provided any evidence that one of ordinary skill in the art would be motivated to modify the line drawing capability already present in Lee. If the proposed combination is an improvement upon Lee, the improvement should be patentable per 35 U.S.C. §101. On the other hand, no evidence has been presented that the proposed combination fixes a recognized problem in Lee. In addition, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[32] Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of clear and particular evidence for motivation to combine the references. As such, claims 11, 13, 25 and 26 are fully patentable over the cited references and the rejection should be reversed.

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[31] Office Action, March 26, 2003, page 7, section 8, line 9.

[32] M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

Selected groupings of the claims are each patentable over Lee, Prouty Krenik and Chiu

12. Group 9 (claim 14) is fully patentable over Lee in view of Prouty, Krenik and Chiu

Claim 14 depends from the claim 11 and thus contains all of the limitations of the claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 (group 8) are incorporated hereunder in support of group 9.

Claim 14 further provides that (i) a first register of the registers is memory mapped to a first location, a second location, a third location and a fourth location in the first address range and (ii) a second register of the registers is memory mapped to a fifth location, a sixth location, a seventh location and an eighth location in the first address range. Despite the assertion by the Examiner, column 10, lines 30-34 of Krenik appear to be silent regarding memory mapping registers to multiple locations.[33] The text of Krenik cited by the Examiner reads:

> a memory having a plurality of locations for storing data and operable to provide a selected portion of said data from a selected one of said locations on a plurality of memory bitlines upon the receipt of an address corresponding to said selected location.

Nowhere in the above text, or in any other section, does Krenik appear to indicate that registers may be memory mapped to multiple locations. Even if the video RAM 20 of Krenik were to be viewed as a collection of multiple registers, nothing is inherent to an arrangement of the video RAM 20 wherein at least two of the registers are each mapped to multiple locations. Therefore, the Examiner has failed to establish that Lee, Prouty, Krenik and Chiu, alone or in combination, teach or suggest a first register of a plurality of registers memory mapped to a first location, a second location, a third location and a fourth location in a first address range and a second register of the registers memory

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[33] Office Action, March 26, 2003, page 5, lines 3-4.

mapped to a fifth location, a sixth location, a seventh location and an eighth location in the first address range as presently claimed.

Claim 14 further provides an address decoder for monitoring the first to the eighth locations. Contrary to the assertion made by the Examiner, column 3, lines 45-49 and elements 122 and 206 in FIG. 2 of Chiu appear to be silent regarding monitoring memory locations.[34] Element 122 of Chiu is a two-conductor control bus.[35] Element 206 of Chiu is an address decoder.[36] The text of Chiu cited by the Examiner reads:

> Address decoder 206 is a binary decoder which produces a load signal on one of four outputs by decoding a two-bit CONTROL signal from decoder 108. The load signals load data from bus 120 into one of the latches 202, 208, 212 and 216.

Nowhere in the above text, or in any other section, does Chiu appear to mention that the address decoder 206 monitors multiple address locations. To the contrary, the address decoder 206 of Chiu appears to control the latches 202, 208, 212 and 216 instead of monitoring the latches. Furthermore, the two control signals received by the address decoder 206 of Chiu can only generate four (not eight) different combinations. As such, the address decoder circuit 336 of Chiu does not appear to be operational to monitor eight locations. Therefore, the Examiner has failed to show that Lee, Prouty, Krenik and Chiu, alone or in combination, teach or suggest an address decoder for monitoring a first to an eighth location as presently claimed.

Claim 14 further provides that the address decoder indexes a style counter in response to the address location being written to. However, the Examiner has not provided any arguments

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[34] Office Action, March 26, 2003, page 8, section 9, line 6 thru page 9, line 1.

[35] Chiu, column 2, line 33.

[36] Chiu, FIG. 2.

or any evidence that Lee, Prouty, Krenik and/or Chiu teach or suggest that the address decoder 206 can index a style counter. Therefore, the Examiner has failed to establish that Lee, Prouty, Krenik and Chiu, alone or in combination, teach or suggest an address decoder indexing a style counter in response to an address location being written to as presently claimed. As such, claim 14 is fully patentable over the cited references and the rejection should be reversed.

Groups 1-14 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[37] As such, each of the above groups is considered to be separately patentable over every other group.[38] In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Group 2 includes an argument that Lee does not disclose or suggest a clipping circuit as presently claimed. Since group 1 does not depend on the clipping circuit argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that Lee and Ashburn do not teach or suggest inhibiting writing data to memory as presently claimed. Since groups 1 and 2 do not depend on the inhibiting argument, group 3 may be found patentable even if groups 1 and/or 2 are not.

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[37] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[38] M.P.E.P., Eighth Edition, Revised February 2003, §1206.

Group 4 includes an argument that Lee and Ashburn do not teach or suggest preventing a calculation of an address as presently claimed. Since groups 1-3 do not depend on the preventing argument, group 4 may be found patentable even if groups 1, 2 and/or 3 are not.

Group 5 includes an argument that Lee and Foley do not teach or suggest discarding data as presently claimed. Since groups 1-4 do not depend on the discarding argument, group 5 may be found patentable even if groups 1-3 and/or 4 are not.

Group 6 includes an argument that Lee and Krenik do not teach or suggest memory mapping as presently claimed. Since groups 1-5 do not depend on the memory mapping argument, group 6 may be found patentable even if groups 1-4 and/or 5 are not.

Group 7 includes an argument that Lee, Krenik and Chiu do not teach or suggest monitoring memory locations for a write. Since groups 1-6 do not depend on the monitoring argument, group 7 may be found patentable even if groups 1-5 and/or 6 are not.

Group 8 includes an argument that there is no motivation to combine Lee and Prouty. Since groups 1-7 do not depend on the motivation argument, group 8 may be found patentable even if groups 1-6 and/or 7 are not.

Group 9 includes an argument that Lee, Prouty, Krenik and Chiu do not teach or suggest an address decoder indexing a style counter as presently claimed. Since groups 1-8 do not depend on the indexing argument, group 9 may be found patentable even if groups 1-7 and/or 8 are not.

Group 10 includes an argument that Lee and Ozcelik do not teach or suggest a control circuit for controlling a register and a calculation circuit as presently claimed. Since groups 1-9 do

not depend on the controlling argument, group 10 may be found patentable even if groups 1-8 and/or 9 are not.

Group 11 includes an argument that Lee and Ozcelik do not teach or suggest storing data in a single memory word prior to the single memory word being written to an address in a memory as presently claimed. Since groups 1-10 do not depend on the storing argument, group 11 may be found patentable even if groups 1-9 and/or 10 are not.

Group 12 includes an argument that Lee and Ozcelik do not teach or suggest combining data for at least two pixels as presently claimed. Since groups 1-11 do not depend on the combining argument, group 12 may be found patentable even if groups 1-10 and/or 11 are not.

Group 13 includes an argument that Lee and Ozcelik do not teach or suggest comparing word addresses as presently claimed. Since groups 1-12 do not depend on the comparing argument, group 13 may be found patentable even if groups 1-11 and/or 12 are not.

Group 14 includes an argument that Lee and Ozcelik do not teach or suggest a control circuit configured to combine data for pixels. Since groups 1-13 do not depend on the control circuit combining argument, groups 14 may be found patentable even if groups 1-12 and/or 13 are not.

C. CONCLUSION

Lee does not disclose or suggest (i) a bus having a first address range and a second address range, (ii) storing coordinates within the first address range, (iii) a memory within the second address range, (iv) calculating an address in the second address range and (v) controlling writing of the data in the memory at the address as arranged in the present independent claims 1, 20 and 30. Lee and Ozcelik, alone or in combination, do not teach or suggest (i) a register accessible via a bus

for storing coordinates of a pixel to be drawn on a display and a memory accessible via the bus for storage of data corresponding to the pixel and (ii) a control circuit for controlling the register and a calculation circuit to cause the data corresponding to the pixel to be stored in the memory at the address as presently claimed in independent claim 15. Furthermore, the Examiner has failed to provide clear and particular evidence of motivation to combine Lee and Ozcelik in regards to claim 15. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered anticipated or obvious by the cited references. However, should the Board find the arguments herein in support of independent claims 1, 15, 20 and/or 30 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a bus having a first address range and a second address range;

a plurality of registers within said first address range configured to store an X coordinate and a Y coordinate of a pixel to be drawn on said display;

a memory within said second address range;

a calculation circuit configured to calculate an address in said second address range for storage of data corresponding to said pixel in dependence on said X and said Y coordinates; and

a control circuit configured to control writing of said data in said memory at said address.

3. The apparatus as claimed in claim 1, further comprising:

a clipping circuit for (i) comparing said X and said Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate that at least one of said X and said Y coordinates falls outside said predetermined clipping limits.

4. The apparatus as claimed in claim 3, wherein said control circuit is further configured to inhibit writing of said data to said address in response to said clipping signal.

5. The apparatus as claimed in claim 3, wherein said control circuit is further configured to prevent calculation of said address in response to said clipping signal.

6. The apparatus as claimed in claim 3, wherein said data is discarded when at least one of said X and said Y coordinates fall outside said predetermined clipping limits.

7. The apparatus as claimed in claim 1, wherein (i) a first register of said registers is memory mapped to a first location and a second location in said first address range and (ii) a second register of said registers is memory mapped to a third location and a fourth location in said first memory range.

8. The apparatus as claimed in claim 7, wherein said apparatus further comprises:

an address decoder for (i) monitoring said first, said second, said third and said fourth memory locations and (ii) applying a location signal to said control circuit representative of an address location being written to.

9. The apparatus as claimed in claim 8, wherein said control circuit is further configured to control said first and said second registers and said calculation circuit in response to said location signal.

10. The apparatus as claimed in claim 9, wherein said control circuit is further configured to instruct said calculate circuit to calculate said address in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

11. The apparatus as claimed in claim 1, further comprising:

a style table for storing data corresponding to a predetermined pattern for said pixel; and

a style counter for (i) indexing said data in said style table and (ii) generating a style data signal corresponding to said indexed data.

13. The apparatus as claimed in claim 11, wherein said style table is configured to store a non-repeating bit pattern up to a predetermined length for a drawing operation.

14. The apparatus as claimed in claim 11, wherein (i) a first register of said registers is memory mapped to a first location, a second location, a third location and a fourth location in said first address range and (ii) a second register of said registers is memory mapped to a fifth location, a sixth location, a seventh location and an eighth location in said first address range; and

said apparatus further comprising an address decoder for (i) monitoring said first to said eighth locations, (ii) generating a location signal representative of an address location being written to and (iii) indexing said style counter in response to said address location being written to.

15. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register accessible via a bus for storing coordinates of a pixel to be drawn on said display;

a calculation circuit for calculating an address in a memory accessible via said bus for storage of data corresponding to said pixel in response to said coordinates; and

a control circuit for controlling said register and said calculation circuit to cause said data to be stored in said memory at said address, wherein said calculation circuit is configured to output said address in a first part and a second part, said first part comprising a word address corresponding to said address in said memory and representing a single memory word and said second part comprising a bit address representing a position of said pixel data within said single memory word.

16. The apparatus as claimed in claim 15, further comprising:

a second register for storing said pixel data in said single memory word prior to said single memory word being written to said address in said memory; and

a multiplexer for writing data to said register in dependence on said address calculated by said calculation circuit.

17. The apparatus as claimed in claim 16, wherein said multiplexer combines data for at least two pixels to be drawn in dependence on said address of each of said pixel to permit storage of said data for said pixels in said single memory word.

18. The apparatus as claimed in claim 17, further comprising:

a comparator connected to said calculation circuit for (i) receiving said addresses, (ii) comparing said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said addresses are identical.

19. The apparatus as claimed in claim 18, wherein said control circuit is further configured to combine said data for said pixels in response to a receipt of said same address signal.

20. A method of generating a region of graphics on a display, the method comprising:

(A) storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

(B) storing a Y coordinate for said pixel in said first address range;

(C) calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

(D) controlling writing of said data in a memory at said address.

21. The method as claimed in claim 20, further comprising:

comparing said X and said Y coordinates with predetermined clipping limits; and

discarding said pixel data in response to at least one of said X and said Y coordinates exceeding said predetermined clipping limits.

22. The method as claimed in claim 20, further comprising:

memory mapping a first register storing said X coordinate to a first location and a second location in said first address range; and

memory mapping a second register storing said Y coordinate to a third location and a fourth location in said first address range.

23. The method as claimed in claim 22, further comprising:

monitoring said first, said second, said third and said fourth locations for a write.

24. The method as claimed in claim 23, further comprising:

calculating said address for said pixel in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

25. The method as claimed in claim 20, further comprising:

storing style data corresponding to a predetermined pattern for said pixel;

indexing said style data; and

generating a style data signal corresponding to said style data as indexed.

26. The method as claimed in claim 25, further comprising:

selecting a color for said pixel to be drawn in dependence on said style data signal.

27. The method as claimed in claim 20, further comprising:

storing said data in a single memory word prior to said single memory word being written to said address in said memory in dependence on the word address or a bit address.

28. The method as claimed in claim 20, further comprising:

combining data for at least two pixels to be drawn in dependence on a word address of each of said pixels to permit storage of said data for said pixels in a single memory word.

29. The method as claimed in claim 28, further comprising:

comparing said word address of consecutive pixels to be drawn; and

combining said data for said pixels if said word addresses are identical.

30. an apparatus for generating a region of graphics on a display, the apparatus comprising:

means for storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

means for storing a Y coordinate for said pixel in said first address range;

means for calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

means for controlling writing of said data in a memory at said address.